IN THE CLAIMS:

Please **SUBSTITUTE** the following claim set for the existing claim set. Claims 1, 5, 6, 15, 19 and 20 have been amended. Please cancel claims 4, 8-14 and 18 without prejudice and please add claims 21-28. A marked up copy of the amended claims with all changes is supplied in the Appendix:

Please cancel claims 4, 8-14 and 18.

We Claim:

1. (Once Amended) An integrated circuit package comprising:

an integrated circuit die, said integrated circuit die having a top side and a bottom side opposite said top side, said top side including at least one bond pad;

at least one raised interconnect located over and conductively coupled to said at least one bond pad; and,

a flexible dielectric circuit film having a top surface, a bottom surface and a routing conductor, the flexible circuit film having at least one outer landing formed on the top surface and at least one inner landing formed on the bottom surface such that the landing on the top surface is fully supported by the underlying circuit film and the landing on the bottom surface is fully supported by the overlying circuit film, wherein the outer landing is laterally offset from the inner landing and the two landings are connected via the routing conductor, the flexible circuit film being located over and conductively attached to at least one raised interconnect such that an air gap is formed between said integrated circuit die and said flexible circuit film.

2. The integrated circuit package of claim 1 wherein said air gap has a height in the range of between about 10μm to 500μm.

3. The integrated circuit package of claim 1 wherein said flexible circuit film is substantially the same size as said integrated circuit die.

5. (Once Amended) The integrated circuit package of claim 1 wherein said outer landing is offset a horizontal distance from said inner landing, and further wherein said horizontal distance in the range of between about 50μm to 1,000μm.

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6. (Once Amended) The integrated circuit package of claim 1 further comprising at least one contact bump conductively coupled with said outer landing of said flexible circuit film.

Sub C1

7. The integrated circuit package of claim 1 further comprising an under bump pad formed over said bond pad and conductively coupled to said at least one bond pad and said at least one raised interconnect.

Sub B2

15. (Once Amended) An integrated circuit wafer having a top side and a bottom side opposite said top side, said integrated circuit wafer comprising:

a plurality of integrated circuit dice, said plurality of integrated circuit dice having a plurality of bond pads located on said top side of said integrated circuit wafer;

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a plurality of raised interconnects formed over and conductively coupled to said plurality of bond pads; and,

a flexible dielectric circuit film having a top surface, a bottom surface and routing conductors, the flexible circuit film having a plurality of outer landings located on the top surface and a plurality of inner landings located on the bottom surface such that the landings on the top surface are fully supported by the underlying circuit film and the landings on the bottom surface are fully supported by the overlying circuit film, wherein the individual outer landings are laterally offset from the individual inner landings and the landings are connected via routing conductors, the flexible circuit film being located over and conductively attached to the plurality of raised interconnects such that an air gap is formed between said integrated circuit wafer and said flexible circuit film.

16. The integrated circuit wafer of claim 15 wherein said air gap has a height in the range of between about 10μm to 500μm.

Sub C1

17. The integrated circuit wafer of claim 15 wherein said integrated circuit wafer further comprises a plurality of under bump pads formed over and conductively coupled to each of said plurality of bond pads.

19. (Once Amended) The integrated circuit wafer of claim 15 wherein each of said plurality of outer landings are offset a horizontal distance from a corresponding one of said inner landings, and further wherein said horizontal distance is in the range of between about 50μm to 1,000μm.

20. (Once Amended) The integrated circuit wafer of claim 15 further comprising a plurality of contact bumps formed on and conductively coupled with said outer landings of said flexible circuit film.

21. (New) An integrated circuit package as recited in claim 1 wherein the flexible dielectric circuit film is made up of multiple layers.

22. (New) An integrated circuit package as recited in claim 1 wherein the flexible dielectric circuit film contains at least one outer landing connected to at least one inner landing via a routing connector in such a way as to form a cantilever-like structure.

23. (New) An integrated circuit package as recited in claim 1 wherein the routing conductor is integrally incorporated into the flexible circuit film such that it is embedded in a dielectric material.

24. (New) An integrated circuit package as recited in claim 1 wherein the routing conductor is integrally incorporated into the flexible circuit film and is formed on one of the top and bottom surfaces of a dielectric material.

25. (New) An integrated circuit wafer as recited in claim 15 wherein the flexible dielectric film is made up of multiple layers.

26. (New) An integrated circuit wafer as recited in claim 15 wherein the flexible dielectric circuit film contains a plurality of outer landings connected to a plurality of inner landings via routing connectors in such a way as to form a plurality of cantilever-like structures.

27. (New) An integrated circuit wafer as recited in claim 15 wherein the routing conductors are integrally incorporated into the flexible circuit film such that they are embedded in a dielectric material.

28. (New) An integrated circuit wafer as recited in claim 15 wherein the routing conductors are integrally incorporated into the flexible circuit film and is formed on one of the top and bottom surfaces of a dielectric material.